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REMARKS

Applicant has also amended claims 10 and 25 for clarity. Claims 1-27 are currently pending.

The Examiner has required election to a species for prosecution on the merits from the following:

Figs. 1-3 and 6-11	Species I
Figs. 4-5	Species II
Figs. 12-13	Species III
Fig. 15	Species IV

In response to the Examiner's election requirement, the applicants hereby elect Species I, Figs. 1-3 and 6-11. Applicant believes that at least claims 1-3, 5, 10-11, 18-20 and 23-26 are readable on Species I. Applicant does not agree with the Examiner that no claims are generic to multiple species.

Attached hereto is a marked-up version of the claim changes made by the present amendment. The attached page is captioned "Version with markings to show changes made."

In view of the above, examination of the present application on the merits is respectfully requested. Should the Examiner wish to discuss this application, the Examiner is requested to call the undersigned at the telephone number listed below.

Respectfully submitted,

Dated: January 16, 2003

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CERTIFICATE OF TRANSMISSION

I hereby certify that this correspondence is being transmitted by facsimile to the United States Patent & Trademark Office at facsimile number (703) 872-9318 on January 16, 2003.

Alan S. Raynes — **January 16, 2003** **Date**

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Version With Markings to Show Changes Made

Claims 10 and 25 were amended as follows:

10. (amended) A semiconductor device having a non-volatile memory transistor, comprising a non-volatile memory transistor including a semiconductor layer, a floating gate disposed above the semiconductor layer, and a control gate formed to extend above a portion of the floating gate, wherein a conduction layer is provided vertically above the floating gate at least in a region where the control gate is not disposed vertically above the floating gate.

25. (amended) A method for manufacturing a semiconductor device having a non-volatile memory transistor, comprising:

forming a floating gate above a semiconductor layer;

forming a control gate that extends above a portion of the floating gate; and

forming a conduction layer vertically above the floating gate at least in a region where the control gate is not disposed vertically above the floating gate.